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Thin Film Deposition, Patterning, and Printing in Organic Thin Film Transistors

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Organic thin film transistors (OTFTs) will play an important role in future plastic electronic devices. The device performance is greatly affected by the molecular structure and morphology of the organic semiconductors. Various methods for organic semiconductor deposition are reviewed. Recent progress in printing and patterning of OTFTs are also surveyed.

I. Introduction

Since John Bardeen, William Shockley, and Walter Brattain invented the world's first transistor in 1947, thin film transistors made of inorganic semiconductor materials, such as silicon and gallium arsenide, have dominated the mainstream electronics industry. However, processing methods for fabricating modern semiconductor devices are becoming increasingly more complex, which correspondingly result in higher production cost.

The first organic thin film transistor (OTFT) was reported in 1986.[2] The motivation came from their easy processibility (low-temperature deposition and solution processing) and flexibility of organic materials. Currently, OTFTs have already shown promising applications in electronic papers,[3−5] sensors,[6,7] and radio frequency identification cards (RFIDs).[8,9]

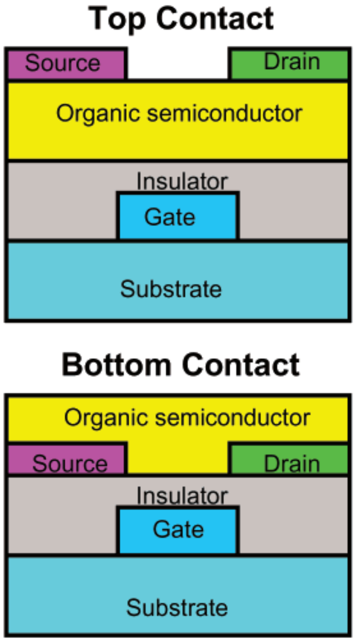

Figure 1. Typical device structures of OTFTs: top-contact and bottom-contact.

Typical OTFT device structures are shown in Figure 1. Source and drain electrodes can be evaporated onto the organic semiconductor layer by way of top contact. Alternatively, organic semiconductors can be deposited onto the already patterned source and drain electrodes to give bottom contact geometry. Contrary to the bipolar junction transistor (BJT), which is a current-controlled device, an OTFT device is essentially a voltage-controlled device. It can operate as a basic "on" and "off" switch, depending on whether a voltage bias is applied at the gate electrode or not. Therefore, it can realize logic functionalities of either "1" or "0". There are two types of OTFTs: (1) The n-OTFT with the major charge carriers being electrons. An n-type channel can be formed at the interface between the organic semiconductor and the dielectric layer. Once this channel is formed, current can pass from the source electrode to the drain electrode. And (2) the p-OTFT with the major charge carriers being holes.

It is known that the performance of OTFTs depends on the construction of each of the active layers, which are the organic semiconductor layer, the insulating (dielectric) layer, and the electrodes. The deposition

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method, condition, sequence, postdeposition treatment, and surface treatment significantly impact OTFT performance. Therefore, it is important to fully understand various factors that affect the thin film growth processes. Specifically, one needs to pay attention to how the molecular structure of the organic semiconductor and thin film morphology affect the performance of OTFT devices, namely, the field effect mobility and on/off ratio.

This review intends to summarize recent progress on methods for thin film deposition and pattern formation for OTFTs. Following an introduction in section I, methods for organic semiconductor thin film deposition are presented in section II. The effects of the surface chemical functionalities and surface treatment on the organic semiconductor thin film growth will be discussed in section III. Methods for patterning and printing are surveyed in section IV. Finally, a summary in section V will conclude this review.

II. Semiconductor Deposition Methods

In this section, various semiconductor deposition methods are discussed. In general, organic semiconductors are deposited either from vapor or solution phase depending on their vapor pressure and solubility. As mentioned earlier, device performance is greatly influenced by various deposition conditions due to the different resulting molecular structure and thin film morphology. Organic materials tend to pack into either a herringbone (for example, α-6T[10]) or a $\pi-\pi$ stacking structure (for example, bis(benzodithiophene)[11]), governed by intermolecular interactions. Better overlap between the π molecular orbitals generally results in a higher mobility, as suggested by quantum chemical calculations.[12] To achieve high field effect mobility, the semiconducting molecules should have an orientation in which the $\pi-\pi$ stacking direction between molecules is arranged in the same direction as that of the current flow. Moreover, larger grain sizes and smooth grains usually tend to give better mobilities.[13] It is known that the current flow in an organic field-effect transistor (OFET) is mainly confined in the first 50 Å of semiconductor layer away from the semiconductor/dielectric interface.[14] The typical semiconductor thickness required for an OFET is in the range of 200−500 Å. A thinner film may have incomplete surface coverage. For bottom-contact devices, a thicker semiconductor layer usually does not affect the charge carrier mobility even though the device off-current may increase for materials with a higher unintentional doping. For top-contact devices, a thicker layer may lead to higher resistance for the charge carriers to travel from the source electrode to the semiconductor/dielectric interface, where the majority of the current flow occurs.

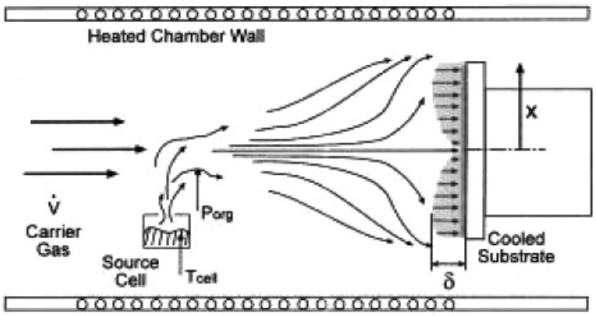

Figure 2. Schematic diagram of OVPD. Reprinted with permission from ref 1. Copyright 2001 American Institute of Physics.

1. Vacuum Deposition. Vacuum thermal evaporation involves heating the organic semiconductor using a resistive heating source under a vacuum environment with a pressure in the range of 10^{-8} to 10^{-6} Torr. For organic small molecules and oligomers that are solution-insoluble, vacuum thermal evaporation is an ideal deposition method. A number of organic semiconductors have been deposited using this method. Examples are oligothiophene and oligofluorene derivatives,[15−17] metallophthalocyanines,[13,18] and acenes (pentacene and tetracene).[19−25] Currently, the best mobility for organic semiconductors has been reported for vacuum-deposited pentacene films.[19,20,23] Vacuum thermal evaporation has the advantages of forming films with high film uniformity and good "run-to-run" reproducibility. Multilayer deposition and co-deposition of several organic semiconductors are possible without the concerns of delamination or dissolution of the previous layers during subsequent deposition steps. However, this method has a relatively high material consumption and also a high initial cost for equipment setup. Nevertheless, this method has already been used for the manufacturing of organic small molecule based light emitting displays by several companies.

Other vacuum based thin film deposition methods employed for OFET fabrication include: organic vapor phase deposition (OVPD), organic molecular beam deposition (OMBD), and laser evaporation. Organic vapor phase deposition (Figure 2) proceeds by evaporation of the molecular source material into a stream of hot inert carrier gas such as nitrogen or argon, which then transports the vapor toward a cooled substrate

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where condensation of the organics occurs.[1,26] With typical conditions used, the flow of the carrier gas around the substrate creates a hydrodynamic boundary layer where molecular transport is diffusion limited. The deposition rate, deposition efficiency, and film morphology are controlled by adjusting the organic species concentration, flow hydrodynamics, and surface diffusivity.[26,27] Since the flow patterns may be engineered, the advantages of this approach include substrate-selective deposition and uniform distribution of organic vapors resulting in a very uniform coating thickness with minimized waste of materials. It has been used to prepare multiplayer organic light-emitting diode (OLED) devices.[28−30] Recently, pentacene films have been prepared using OVPD and their transistor performance hase been investigated.[27] Performance similar to films prepared by vacuum thermal evaporation was obtained.

Evaporation of organic materials in an ultrahigh vacuum (UHV) is sometimes referred to as organic molecular beam deposition (OMBD) or organic molecular beam epitaxy (OMBE).[31] Monolayer control over the growth of organic thin films with extremely high chemical purity and structural precision is possible with this deposition method. This method can be combined with in situ high-resolution structural diagnostic tools as the films are being deposited and allows for understanding of the fundamental structural and optoelectronic properties of ultrathin organic film systems. It has been used for deposition of pentacene OFETs, and was observed to give a mobility of 0.038 cm^2/Vs.[32] This lower mobility compared to those obtained with typical vacuum thermal evaporation may be related to the formation of two pentacene phases at a relatively low evaporation rate typical for OMBD.[32] Gross et al. have successfully grown perylene monolayer on Au(110) using OMBE.[33] Recently, a modified OMBD for organic semiconductors, namely seeded supersonic molecular beam epitaxy (SuMBE) technique[34,35] was reported by S. Iannotta et al. The vapor of the resistively heated raw material was "seeded" in a He carrier gas flowing into a capillary. The molecular precursors in the beams are highly regulated in terms of kinetic energy at the initial state of deposition. This method thus allows good control of the thin film morphology, structure, and functional properties of the resulting films. Oligothiophenes, pentacene, and phthalocyanine films have been deposited by this method.[34,35] Films with high crystallinity were formed attributed to the local annealing induced by the initial kinetic energy of the molecules in the supersonic beam. However, no OFET performance based on films deposited by this method has been reported.

Laser ablation technique, which is widely used for deposition of a variety of inorganic materials, has also been applied to the deposition of organic semiconductors. A pulsed ultraviolet laser is used to induce evaporation as comparable to those produced via thermal evaporation.[36] The vaporized organic semiconductor condenses on a nearby cooled substrate. It was found that laser-deposited pentacene films had properties (such as optical properties, field effect mobilities, and surface morphology) similar to those of the thermally evaporated films.[36] Pentacene films produced this way contain a single-phase with interlamella spacing characteristic of the thin-film phase.[36] This technique has also been used for the deposition of other materials such as poly(ethylene-*alt*-maleic anhydride).[37]

Several factors should be considered when selecting the deposition conditions in order to achieve high OTFT performance. First, deposition rate and substrate temperature directly affect the crystallinity and morphology of the resulting thin film. Second, the substrate surface onto which the organic semiconductor materials are deposited also has a great impact on the formation of the thin film, and thus the performance of the resulting device. Finally, postdeposition treatments, such as annealing, may further improve device performance and characteristics. Even though different vapor phase deposition methods may be used, many of the considerations for deposition conditions, surface treatment, and postdeposition annealing are similar. They will be discussed in greater detail later in the following sections.

2. Solution Deposition. Deposition methods based on solution-processable materials are not limited by the size of the vacuum chamber and no pumping down time is required. They are compatible with large-area thin film fabrication and therefore result in lower production cost per device. Solution deposition, such as screen printing and ink jet printing,[38−43] also allows the possibility of printing the active materials in which the deposition and patterning are accomplished in a single step.[44] Two approaches have been used to obtain organic semiconductor thin films from solution: (1) deposition of a soluble precursor from solution and subsequent conversion into the final semiconductor; or (2) direct deposition of a soluble semiconductor.

Most conjugated oligomers and polymers used as semiconductors are insoluble in common solvents unless solubilizing substitutions are incorporated into the

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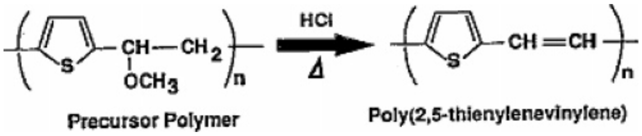
Scheme 1. Conversion Reaction from a Precursor Polymer to Poly(2,5-thienylenevinylene) (PTV) (Reprinted with permission from ref 49; Copyright 1993 American Institute of Physics)



molecular structures. Sometimes, these substitutions may either interfere with molecular packing or increase the $\pi-\pi$ stacking distance between molecules, both of which result in lower charge carrier mobilities. Electrochemical polymerization has been used to synthesize and deposit polythiophene semiconductor directly into the channel region.[2] However, polymers prepared this way tend to be partially doped and usually have low on/off ratios. In addition, the field-effect mobility of this polymer is low because it is partially cross-linked during the polymerization process and results in poor molecular ordering. To overcome these problems, several groups have taken the approach of synthesizing soluble precursors which can subsequently be converted into the final semiconductor after film deposition from solution. Pentacene transistors with high mobilities have been reported using this approach.[45–47] Oligothiophene and poly(thienylene vinylene) transistors have also been prepared with reasonable mobilities.[48–50] Another interesting example involves deposition of an n-channel ladder polymer from solution using a Lewis acid acting both as a chelating and solubilizing group. After film deposition, the Lewis acid was removed by extensive washing.[51,52] High n-channel mobility was reported with the proper selection of Lewis acid, which results in thin films of highly ordered polymers.[52] However, the catalyst has to be completely removed, otherwise undesired mobile ions may be present in the film and lead to unusual electrical characteristics.[51] As an illustration, the conversion reaction from a precursor polymer to poly(2,5-thienylenevinylene) (PTV) at 200 °C is shown in Scheme 1.[49]

The conversion temperature for precursor materials required for achieving high mobility tends to be high (above 125 °C) and may be incompatible with low-cost plastic substrates. The additional conversion step is also time-consuming. Therefore, direct deposition of soluble semiconductor is more desirable. Both polymers and oligomers have been directly deposited from solution. Polymers tend to have better thin film forming properties with good uniformity over a large area. However, they are more difficult to purify and it is harder to achieve good long-range molecular ordering. The best mobility, in the order of 0.1 cm^2/Vs, is obtained with solution-deposited polymer such as regioregular poly(3-hexylthiophene) (PHT) and a structurally modified derivative.[18,53–56] Much work has been done to study PHT TFTs.[57–61] Oligomers, on the other hand, can be easily purified by column or sublimation. However, they tend to be highly crystalline and thus it is difficult to form a smooth uniform film over a large area. High mobilities have been reported with several oligomers by optimizing the deposition conditions.[62–64]

Both spin-coating and solution-casting are commonly used for solution deposition.[61,65–68] In the spin-coating method, the solvent dries relatively fast allowing less time for molecular ordering compared to that in solution-casting. But the film uniformity is usually better for spin-coated films. These films can be annealed afterward to improve molecular ordering as discussed later. For materials with tendencies to form highly ordered molecular packing, it was found that even spin-coated films can achieve very high mobilities.[53] For example, for regioregular poly(3-hexylthiophene) with 80% regioregularity, the plane of the thiophene rings in the polymer backbone are primarily oriented parallel to the substrate surface (Figure 3b) in the spin-coated film, while the solution-cast film has the thiophene rings perpendicular to the substrate surface (Figure 3a) resulting in an increase of mobility by more than 1 order of magnitude.[53] If the regioregularity was greater than 95%, similar mobilities were obtained with both spin-coated and solution-cast films.[53]

For solution deposition, semiconductor concentration, solvent evaporation rate, solubility of the semiconductor, and the nature of the substrate surface play important roles in the quality of the resulting semiconductor films. The solvent dependence of highly regioregular (>95%) poly(3-hexylthiophene) has been studied.[18,69] It was found that the mobilities of these polymer transistors

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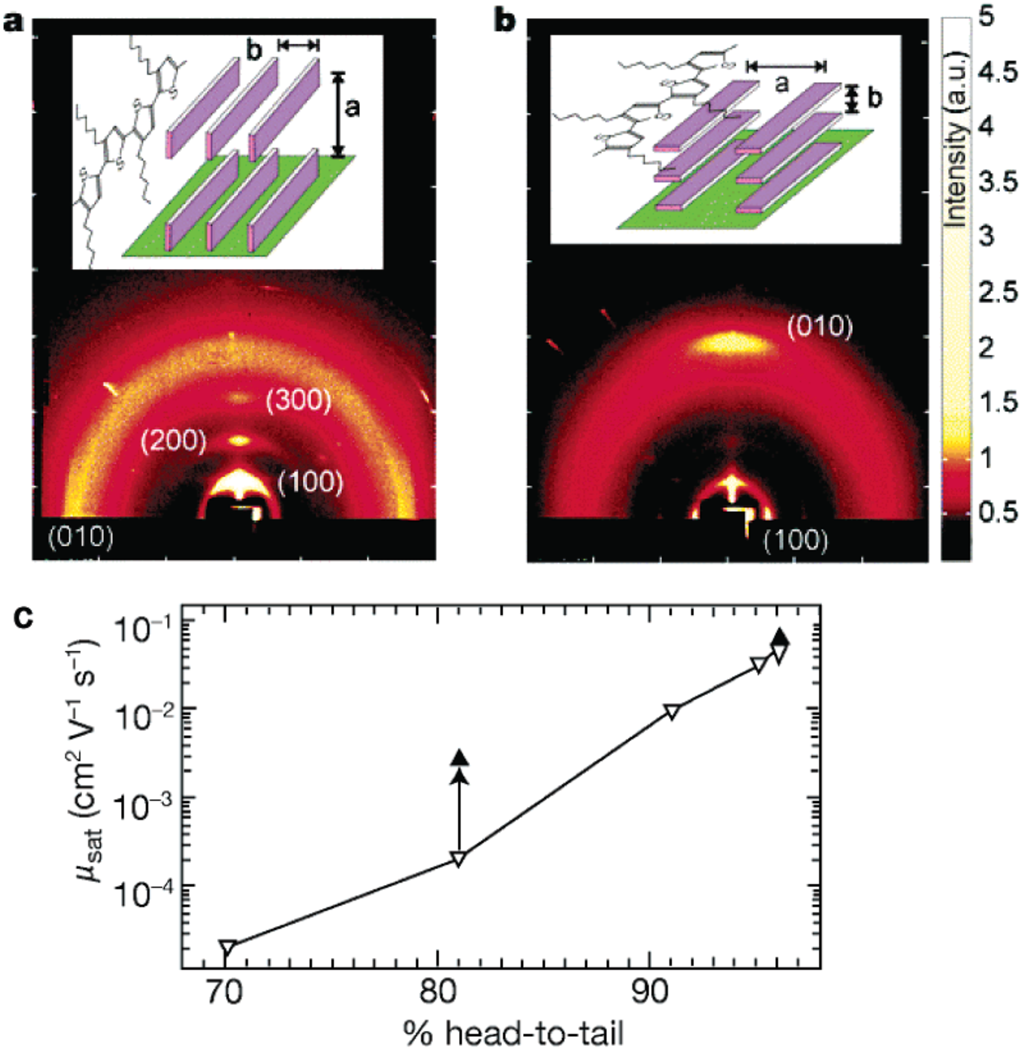

Figure 3. Two different orientations of ordered P3HT domains with respect to the FET substrate. (a and b) The wide-angle X-ray scattering images are a color representation of the two-dimensional distribution of scattered Cu Kα X-ray intensity from spin-coated, 70−100-nm-thick P3HT films with regioregularity of 96% (a) and 81% (b) on SiO_2/Si substrates. (c) Dependence of the room-temperature mobility on the regioregularity for spin-coated (downward triangles) and solution-cast (upward triangles) top-contact P3HT FETs (channel length $L = 75$ μm, channel width $W = 1.5$ mm). Reprinted with permission from ref 53. Copyright 1999 Nature Publishing Group.

are highly dependent on the solvent used for casting films. The best solvent was chloroform, which gives films with densely packed and interconnected nanofibrils morphology.[69] The structure analysis with grazing incidence wide-angle X-ray diffraction (GIWAX) indicated that the polymer conformations are similar regardless of the solvent used for film preparation, i.e., similar polymer orientation as shown in Figure 3a was found for PHT with more than 95% regioregularity. The difference in mobility was thus attributed to the difference in the nanofibrils morphology. When the fibrils are densely packed in the case of chloroform as a solvent, the thin film mobility is higher than that of the loosely packed fibrils that result when methylene chloride is used as the solvent.[69]

For polymer semiconductors, their molecular weight and polydispersity also have great impact on the morphology of their thin films. Recent work has shown that the mobility of spin-coated regioregular poly(3-hexylthiophene) differs by several orders of magnitudes depending on the molecular weight of the polymer.[70] The mobility was found to increase with molecular weight. Low-molecular-weight PHTs (number-averaged molecular weight less than 10 000) were found to form rodlike morphology, whereas high-molecular-weight polymers formed isotropic nodules. It is unclear whether the difference in mobility is due to the sharper interface between rods in the low-molecular-weight films or the fact that the larger-sized molecules require less hopping between molecules.[70]

The Langmuir−Blodgett (LB) technique is another possible method to deposit organic semiconductor thin films.[71−75] LB film is an ordered array of amphiphillic molecules formed by compression with a blade on a water surface. The film can then be transferred onto a

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substrate either as a monolayer or multilayers. The molecules in the LB film are usually well-aligned. OFETs have been fabricated using this technique.[71,72] However, poly(3-hexylthiophene) was used and it is not an amphiphillic polymer. It was therefore difficult to obtain highly aligned monolayer films on an air−water interface. Mobility similar to that of a solution-cast film was obtained with little anisotropy in the film even though optical anisotropy was observed.[72] Surfactant molecules can be incorporated to improve the ordering, but at the same time these insulating molecules disrupted charge transport.[71]

Layer-by-layer deposition of thin films involves dipping a substrate in alternating solutions containing positively and negatively charged polyelectrolyte.[76,77] Greater control over layer thickness and uniformity can be achieved. This method has been used for the fabrication of various organic devices, such as photovoltaic cells and light-emitting diodes.[78−80] Its application in OFETs was explored recently with copper phthalocyanine derivatives substituted with positive and negative charges to allow their deposition using the layer-by-layer approach.[81] The drain-source current was found to be gate-voltage dependent showing similar trends as p-channel and n-channel device characteristics. However, these characteristics disappeared when the devices were measured under vacuum. Therefore, the observed field-effect was attributed to ion-induced field-effect due to the presence of ions in thin films prepared by this method.[81]

3. Effect of Deposition Conditions. *(a) Deposition Rate.* Thin film deposition rate affects the nucleation density of a given organic semiconductor on a given substrate surface. In general, a faster deposition rate leads to higher nucleation density and smaller average grain sizes. An additional energy is required for charge carriers to hop from one grain to another.[82] In addition, impurities and trapping molecules absorbed from the ambient environment tend to accumulate at grain boundaries and further increase the energy barrier for hopping. Therefore, high mobility is generally obtained for films with large and interconnected grains. However, faster deposition rate sometimes results in the formation of a different crystal packing phase which may give improved device performance. For example, some earlier work using molecular beam deposition showed the correlation between the morphology of pentacene thin film and deposition rate using X-ray diffraction and scanning electron microscopy.[32] It was found that two phases coexisted in pentacene thin films: the thermodynamically stable bulk phase and the meta-stable thin-film phase. Mixed phases were obtained at low deposition rates with a substrate temperature of 55 °C. The thin film phase was found to have better mobility than the mixed phases. Lower deposition rates in this case resulted in the formation of the lower mobility mixed phases.

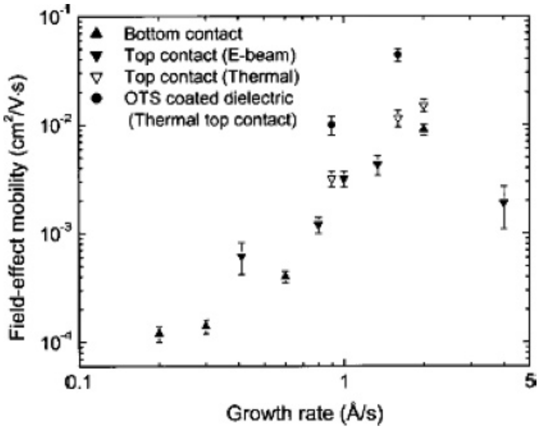

Figure 4. Field-effect mobility of BTQBT organic thin-film transistors as a function of the channel growth rate. The mobility increases with the growth rate as the molecules within the channel becomes more ordered. Reprinted with permission from ref 88. Copyright 2001 American Institute of Physics.

The correlation between charge carrier mobility and deposition rate of pentacene TFTs has been investigated in more detail recently.[83] TFTs with pentacene deposition rates of 1, 3, 5, and 7 Å/s at 25 °C, and 7 Å/s at 60 °C were prepared. It was found that the field-effect mobility increased with deposition rate even though the film became less crystalline compared to the ones deposited at lower deposition rates. With a deposition rate of 7 Å/s at 60 °C, the resulting pentacene TFT had a mobility of 0.3 cm^2/V s and an on/off current ratio of 10^4. Continuous efforts to understand the effects of deposition rate have been made during the past few years.[84−87]

The field-effect mobility of OTFTs based on a planar sulfur-containing organic compound, bis(1,2,5-thiadiazolo)-*p*-quinobis(1,3-dithiole) (BTQBT) deposited using organic molecular-beam deposition, was found to depend on its deposition rate as shown in Figure 4.[88] The mobility increased when the deposition rate was higher because the molecules in the channel had became more ordered. Similar types of studies on other materials systems have also been carried out by the same group.[27]

(b) Effect of Substrate Surface. Substrate surface properties have significant impact on the molecular orientation and thin film morphology of the semiconductor being deposited upon. In most cases, this substrate surface is also the dielectric surface. It is known that the current flow in an OFET is mainly confined within the first 5 nm of semiconductor away from the dielectric/semiconductor interface.[14] Therefore, the mor-

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phology and molecular orientation of this first 5 nm film is most critical to the performance of OFETs. Unfortunately, it is difficult to probe detailed molecular orientation in an ultrathin film. The commonly accepted notion is that the larger the gain size, the higher the mobility due to the reduced number of grain boundaries. However, grain size is usually determined by imaging the surface of organic semiconductor by atomic force microscopy (AFM) or scanning electron microscopy (SEM). In both cases, no information on the morphology of the film at the interface is given and may lead to exceptions from the above commonly accepted notion. For example, it was found that films with smaller pentacene surface grains sometimes gave mobilities several times higher than films with much larger surface grains.[27] Pentacene films were examined by transmission electron microscopy (TEM) and it was found that the electron diffraction pattern within a 10-μm-diameter area of the seemingly multigrain film was single-crystal-like indicating these grains have little mutual mismatches.[89] Recently, GIWAX has been used to study a monolayer of pentacene deposited on amorphous SiO_2, commonly used as a dielectric layer for OTFTs.[90] The results confirm that the monolayer is crystalline and has a structure that differs from that of bulk pentacene.

Both organic and inorganic materials have been used as the dielectric layers for OFETs. The choice of the dielectric material has a significant impact on OFET performance. Different dielectric materials have different surface properties that affect the growth of the organic semiconductor. In addition, some studies suggested that materials with higher dielectric constant may be desirable not only for higher current output,[91] but also for the fact that they allow induction of a higher charge carrier concentration with the same applied gate field. Therefore, shallow traps can be easily filled leaving more access charge carriers available for charge transport.[91] Various inorganic materials such as SiO_2, SiN_x, Al_2O_3, Al_2O_{3+x}, and Ta_2O_5 have been evaluated as gate dielectric layers for OFETs.[92−97] SiO_2, SiN_x, and Al_2O_3 film depositions usually require high substrate temperatures (about 250 °C) and therefore are not compatible with low-cost plastic substrates. It was reported that Al_2O_{3+x} film deposited on indium−tin-oxide (ITO) glass at room temperature can be used as gate dielectric layer.[98,99] The film gave a moderately high pentacene field mobility of 0.14 cm^2/Vs, an outstanding subthreshold slope of 0.88 V/dec, and an on/off ratio over 10^6.[98,99] Its dielectric constant has a value of about 7, and the breakdown field is about 3 MV/cm.[98,99] An anodization method was reported to give high-quality oxide (for example tantalum oxide and silicon dioxide) dielectrics on gate electrodes of certain metals (such as Ti, Zr, Hf, Nb, Ta, and Al) and doped Si.[100] Tantalum oxide is chosen due to its high dielectric constant ($\epsilon \approx 23$) and low electrical leakage ($<10^{-8}$ A/cm^2 at 1 MV/cm). Working transistors with reasonable performance were reported.[100]

Polymer dielectric layers have also been widely investigated,[101−103] although their dielectric constants are usually low.[104] Polymer dielectrics have several advantages: they have good insulating properties and high intrinsic breakdown voltage; they can undergo plastic deformation in the presence of external stress, thus reducing residual stress in the dielectric films; and most polymers are solution processable by spin-coating or printing. The limitation is that they may not be compatible with high-temperature processing conditions. A number of polymer dielectric materials have been investigated in the literature.[102,105,106] A few dielectric polymers have been found to give good transistor performance for a variety of different organic semiconductors. Some examples are polyvinyl phenol,[23,50] cross-linkable polyvinyl phenol,[23] polystyrene, glass resin,[102] and polymethyl methacrylate (PMMA).[105,107] Besides having a low surface trapping density, an extremely flat (or low roughness) dielectric surface achievable by spin-coating is important for the growth of large crystalline grains. Rough surfaces tend to result in high nucleation density. They can also act as scattering sites for charge carrier transport. Large pentacene single microcrystals were grown directly on PMMA surface and mobility as high as 1.2 cm^2/Vs was obtained with these OFETs.[107]

(c) Effect of Surface Treatment. Surface treatment of dielectric layer is an important way to improve OFET performance. While the dielectric constant and leakage current are determined by the bulk properties of the selected dielectric material, the device performance is largely affected by the surface properties of the dielectric layer. The dielectric surface can be modified to improve the growth of the organic semiconductor (i.e., larger and smoother grains or macroscopic alignment of molecules) and reduce trapping densities. For inorganic oxide surfaces, different surface modification chemistries have already been well-developed and can be easily adapted. For example, SiO_2 surface has been modified with hexamethyldisilazane (HMDS) to reduce trapping by Si−OH.[40] Capping SiO_2 surface with octadecyl trichlorosilane (OTS) not only removes Si−OH trapping centers,

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but also leads to larger grain growth and improved crystalline ordering.[20] Pentacene field-effect mobilities between 0.6 and 2.1 cm²/Vs have been obtained for OTFTs using OTS-treated silicon dioxide layer, better than those without OTS treatment.[27] OTS treatment has also been carried out for cross-linked poly(4-vinylphenol) (PVP) dielectric layer TFTs.[108] Al_2O_3 dielectric surface has been modified with alkane phosphonic acids, and very high pentacene mobilities (1−3 cm²/Vs) were reported.[19] An impressive pentacene mobility of 7 cm²/Vs, exceeding the highest mobility value recorded for pentacene single crystals, was recently reported by the group at 3M Corp.[109]

The growth dynamics of pentacene thin films on Si and SiO_2 surfaces were studied using the real-time imaging capability of photoelectron emission microscopy.[110] With a clean Si(001) surface, a dead time at the initial growth was found associated with pentacene lying flat on a clean H atom terminated Si(001) surface. Removal of the reactive dangling bonds by absorption of cyclopentene or the use of SiO_2 resulted in no initial dead time. In all three cases, the highly uniform surface led to much lower nucleation density (i.e., larger grains) than previously reported. Single-crystal grain sizes approaching 0.1 mm at room temperature were obtained on these surfaces.[110]

The nucleation of pentacene on reduced and oxidized silicon surfaces was studied with the help of AFM and X-ray reflectivity measurements.[111] Three types of surfaces were prepared: a clean SiO_2 surface with hydrophilic termination, a reduced hydrophobic H atom terminated Si surface, and a chemically reoxidized hydrophilic SiO_2 surface. It was found that the morphology of the first layer of pentacene was strongly influenced by the surface termination groups. A reduced H atom terminated surface was favored for the growth of larger grains. Another interesting finding is that the first one and two layers of pentacene film had a reduced mass (75% of bulk film density) indicating reduced molecular packing efficiency at the beginning of pentacene growth.[111] A photoemission electron microscopy study on nucleation of pentacene films on both SiO_2 and Si(001) has also been carried out recently.[86]

Interfacial chemistry of pentacene on clean and chemically modified Si(001) surfaces has been studied.[112] The interactions between pentacene and Si(001) surface were studied using Fourier transform infrared spectroscopy (FTIR). It was found that the first layer of pentacene molecules reacted with Si−H bonds on Si(001) surface. It was also found that pentacene molecules in layers beyond the first layer were adsorbed molecularly and yielded well-defined valence band features.

Theoretical studies of nucleation of organic semiconductors on inert substrates have been reported recently.[113] Simulations of the growth of various materials (pentacene, tetracene, and perylene) on inert SiO_2 and OTS-modified SiO_2 surfaces were performed. Two-dimensional (2D) and three-dimensional (3D) nucleation behavior have been simulated and compared with experimental findings. 2D nucleation is more favorable for charge transport because it leads to the formation of smoother films. Other physical models for organic thin film growth have also been tested.[114,115] Recently, AFM and X-ray studies were performed to determine dynamic scaling, island size distribution, and morphology in the aggregation regime of submonolayer pentacene films.[116] The diffusion-mediated scaling behavior of island size distribution was confirmed.

For polymer insulators, surface modification is most conveniently achieved by using a double layer structure as long as the two layers are carefully chosen so that the deposition of the second layer does not damage the first layer. A water-soluble clay mineral layer was deposited on a PMMA insulating layer before pentacene was deposited.[117] Improvement of the drain current and disappearance of current−voltage hysteresis were reported. Low hysteresis was also found when insulating polymers with low dielectric constants were used.[118] However, for higher current output and faster device operation, high dielectric constant is desirable. The proposed solution was to coat an ultrathin layer of low dielectric constant polymer above a high dielectric constant polymer.

In most organic transistors, the distance between drain and source electrodes is much greater than the size of a single grain, which means the molecules within the channel region do not all have the same orientation. The energy barrier for charge carriers to hop from one grain to another needs to be overcome for the charge transport across the channel. One possible way to improve mobility is to minimize these energy barriers by aligning the molecules with their $\pi-\pi$ stacking direction in the same direction of current flow. This can be achieved by rubbing techniques on the dielectric surface. For example, a rubbed polyimide surface commonly used for the alignment of liquid crystals was used to align pentacene semiconductor even though pentacene does not have liquid crystallinity.[119] A very thin layer of organic semiconductor can be deposited on the dielectric layer and subsequently rubbed gently with a Teflon bar leaving grooves that align the same kind of organic semiconductor deposited above it (Figure 5).[120]

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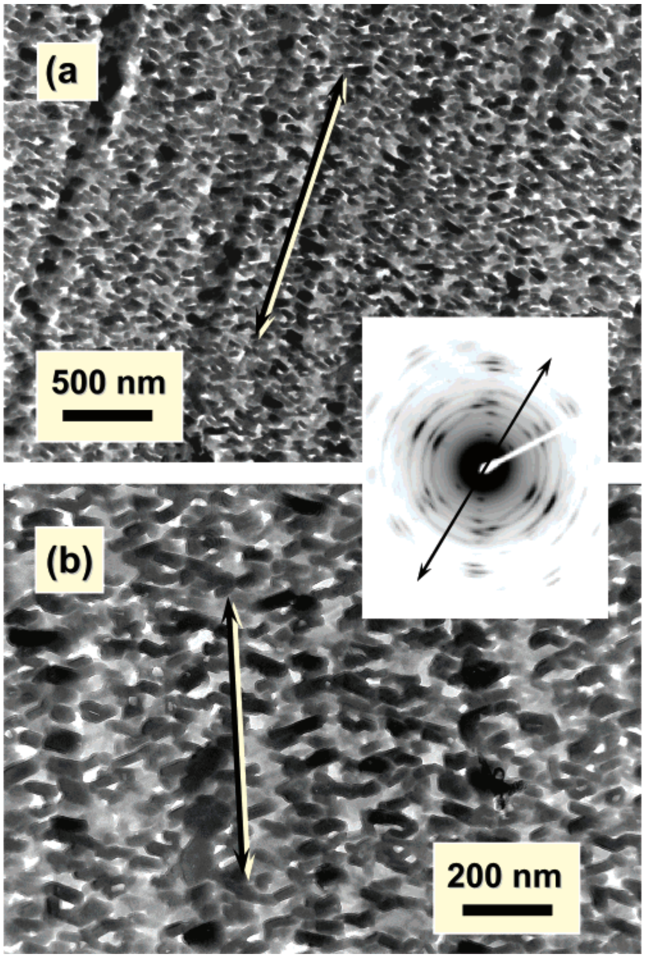

Figure 5. Transmission electron micrographs (at two different magnifications) of rubbed α-sexithiophene (6T) films following subsequent sublimation of 50-nm α-6T. Inset, selected-area electron diffraction pattern from a rubbed α-6T thin film following subsequent sublimation of 50-nm α-6T. Reprinted from ref 120. Copyright 2001 American Chemical Society.

It was found that both the molecules and the grains grown from them were aligned along the rubbing direction. The mobility along the rubbing direction was found to be slightly enhanced (1.5 to 2 times) compared to the untreated films, while the mobility perpendicular to the rubbing direction was several orders of magnitudes lower.[120] The anisotropy was attributed to the roughness induced by rubbing rather than uniaxial alignment of the molecules. A nice device structure that takes advantage of the alignment effect and avoids the roughness at the dielectric−semiconductor interface is to use different layers for the alignment layer and the dielectric layer. In this structure, the dielectric layer is deposited onto the already aligned semiconductor followed by a gate electrode on top.[121] In the cases where the semiconducting material is liquid crystalline, better alignment of the semiconducting molecules can be achieved. In theory, a monodomain without grain boundaries should be achievable and the mobility after such treatment was improved by 1 order of magnitude from 10^{-3} to 10^{-2} cm^2/Vs.[121] It has been demonstrated that (dioctylfluorene)-bithiophene copolymer (F8T2) can be aligned from the nematic liquid-crystalline phase above 265 °C and then subsequently quenched into a monodomain.[122] Enhanced mobility up to 0.01 cm^2/Vs has been achieved. Moreover, the mobility along the rubbing direction was found to be higher than that in the perpendicular direction with anisotropy ratio similar to the optical dichroic ratio.[121] Friction-transferred highly oriented poly(tetrafluoroethylene) (PTFE) has also been used to align various materials ranging from oligomers to polymers. OFETs of regioregular poly(3-hexyl thiophene) have been fabricated on a highly oriented PTFE-treated SiO_2 surface, and mobility along the rubbing direction was found to be much higher than that along the perpendicular direction.[123] Again, the difference was mainly attributed to the surface roughness induced by the PTFE. Such a surface was also used to align discotic derivatives of hexabenzocoronene so that the $\pi-\pi$ overlap direction is along the current flow direction.[124] Without the rubbed PTFE layer, this type of liquid crystalline molecules tends to orient themselves with their molecular planes lying flat on the surface, which does not give high charge carrier mobility. Oriented films of tetracene and pentacene deposited by vacuum sublimation onto friction-transferred PTFE have also been reported.[125]

(d) Electrode Surface Treatment. Optimized grain growth on drain and source electrodes is important for achieving high mobility for bottom-contact geometry. This device structure is convenient for fabrication since the drain and source electrode patterning is carried out before the deposition of the organic semiconductor. Therefore, there is no concern of degradation of the organic semiconductor during electrode fabrication. However, in most cases charge injection is found to be much more efficient with top-contact device structure than with bottom-contact.[126] Gold is typically used as the drain and source material. However, it was found that most organic semiconductors tend to form small grains on gold electrodes. The morphology of organic semiconductors on Au is usually different from that on dielectric surface. This results in an energy barrier for charge carriers to transport from the small grain region to the large grain region and lowers the device performance. Figure 6 shows the scanning electron micrograph of both the channel and the Au electrode regions of a pentacene transistor.[127] It can be seen that pentacene grains are significantly smaller on the electrode region compared to the channel region on SiO_2. Treating the Au surface with a self-assembled monolayer (SAM) of hexadecanethiol resulted in larger pentacene grain growth on Au and improved mobility.[127] In addition to promoting larger grain growth, a SAM can also be chosen to “dope” the semiconductor and improve charge injection. For example, 4-nitrobenzenethiol was used to

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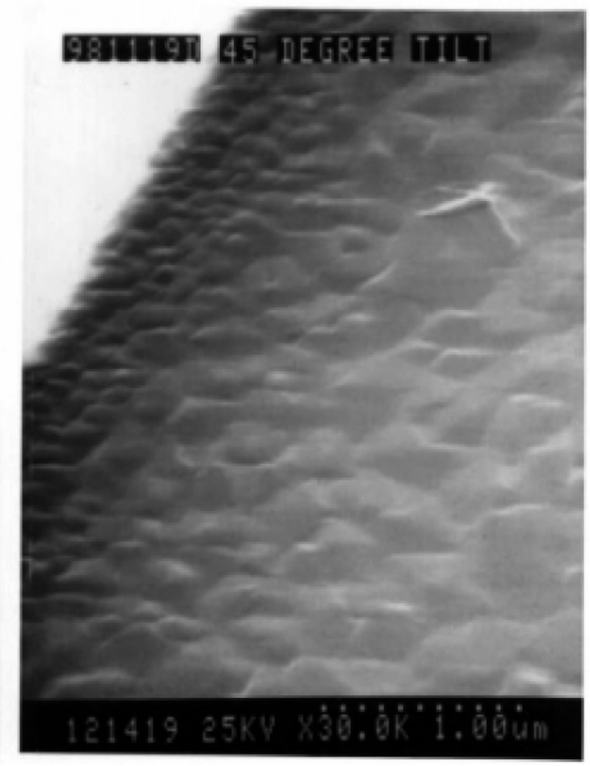

Figure 6. SEM micrograph of a pentacene bottom-contact transistor. The bright region shows the Au electrode region. It can be seen that smaller grains are formed at the Au region while larger grains are found in the SiO_2 region. From the center of the Au toward the center of the channel there exists a transition region of microcrystalline pentacene. This form is believed to be the cause for the inferior performance of bottom-contact pentacene transistors compared to that of top-contact devices. Reprinted with permission from ref 127. Copyright 2001 Institute of Electrical and Electronics Engineers.

modify Au source and drain electrodes, and improved pentacene transistor performance was observed.[128]

For certain organic semiconductors, without Au surface treatments their bottom-contact devices may not be functional at all. For example, several n-channel organic semiconductors showed transistor behavior only after the drain and source electrodes were treated with SAMs.[129] It was not clear whether the improvement in these cases is mainly associated with improved growth of organic semiconductor on the Au drain and source electrodes or due to the improved charge injection through electronic interaction between the SAM and the semiconductor. Recent studies have shown lower charge injection barrier for conducting polymer electrodes than metal (Au) electrodes despite their very similar work functions.[126] The most desirable case is to use SAMs, which improves semiconductor growth as well as having electronic interaction with the semiconductor to favor better charge injection.[128]

(e) Other Parameters. Other methods to obtain large grain size, common to both vapor and solution phase deposition, are increasing substrate temperature during deposition, and postdeposition annealing of the semiconductor films.[130−135] In general, higher substrate temperature during deposition leads to lower nucleation density and larger grains and improved mobilities.[132,133] However, the large grains still need to be intimately connected with each other to favor high mobility.[136] For every semiconductor, there is an optimal substrate temperature that gives the highest mobility where the grain size is large and at the same time the grains are well connected.[136] Figure 7 shows the mobility dependence of copper phthalocyanine TFTs on substrate temperature during deposition. It can be seen that there is a strong correlation between the charge carrier mobility and the substrate temperature.[136] The field-effect mobility increased from 10^{-5} to 10^{-2} cm^2/Vs while the substrate temperature was raised from -100 to 125 °C. At higher substrate temperatures empty gaps formed between grains and lower mobilities were obtained even though the grain sizes were significantly larger. For the simplicity of processing, it is desirable to use unheated or moderately heated substrates. Moreover, cracks may be formed in the semiconductor due to the mismatch of thermal expansion coefficients between the semiconductor and the substrate when high substrate temperature is used during semiconductor film deposition.

Postdeposition annealing is commonly used to improve thin film morphology after deposition. It is most effective for polymers with relatively low glass transition temperatures (T_g) and oligomers with relatively low melting points. Polymer semiconductors can be annealed at around or above glass transition temperatures to improve ordering. For oligomers the annealing has to be done near the melting temperatures. If the semiconductor also has liquid crystallinity (LC), annealing in its LC phase or in conjunction with an alignment layer are effective ways to improve molecular ordering and mobility.[121]

III. Patterning and Printing

Electrode and semiconductor patterning is crucial for the fabrication of OTFTs. Specifically, patterning of organic semiconductors is necessary to eliminate parasitic leakage and reduce cross talk in order to achieve high on/off ratios.[4,137] The drain and source distance, defined as channel length, needs to be less than 10 μm for most applications with OTFTs. The major considerations for patterning are cost, throughput, achievable feature size, and compatibility with organic semiconductors. Various patterning techniques have been developed and they can be categorized into three types:

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(136) Bao, Z.; Dodabalapour, A.; Lovinger, A. *Appl. Phys. Lett.* **1996**, *69*, 3066−3068.

(137) Kyissis, I.; Dimitrakopoulos, C. D.; Purushothaman, S. *J. Vac. Sci. Technol. B* **2002**, *20*, 956−959.

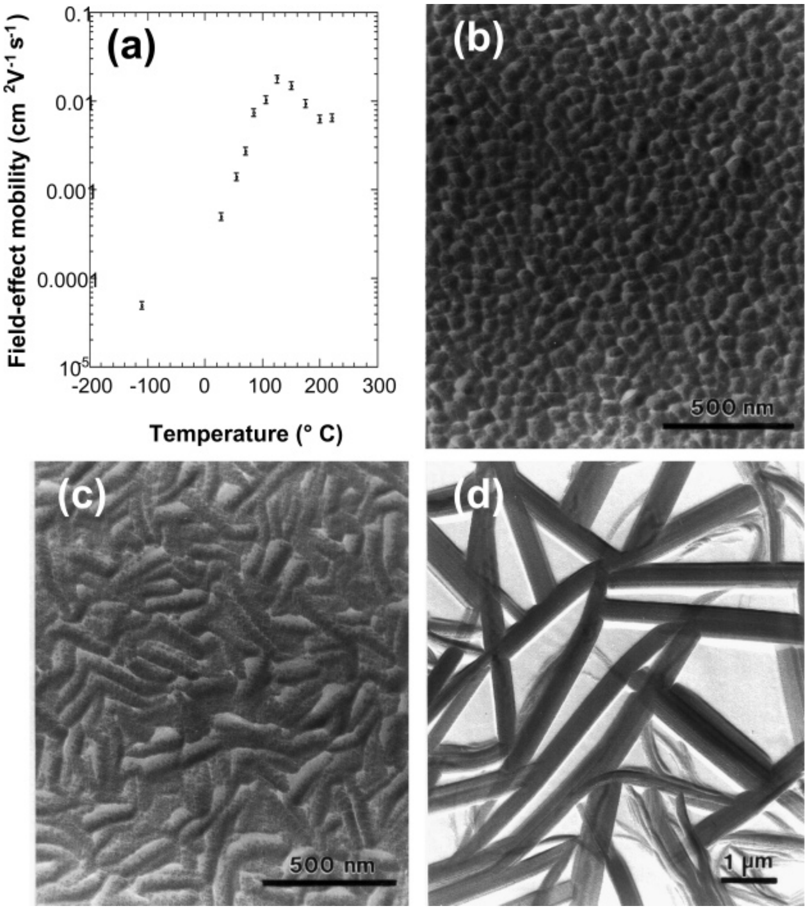

Figure 7. Field-effect mobility of copper phthalocyanine (CuPc) as a function of substrate temperature (a). The grain size of CuPc increases with substrate temperature during deposition. At room temperature (b), the grain size is small and the mobility of this film is low. When the substrate temperature is 125 °C (c), relatively large and densely packed grains are formed. When the substrate temperature is 225 °C (d), large grains are formed together with empty spaces resulting in low charge carrier mobility. Reprinted with permission from ref 136. Copyright 1996 American Institute of Physics.

optical lithography, shadow masking, and printing. Optical lithography is a well-developed conventional technique for the patterning of mesoscopic features and components for microelectronic and photonic devices. It has also been proven useful for OTFT fabrication even though the cost for production may be relatively high. OTFT components can also be formed by depositing relevant materials onto the substrate through shadow masks. Shadow mask patterning is a "dry" process avoiding solvents which could degrade the organic semiconductors. However, the resolution of shadow-masking is limited. Printing methods allow the possibility of depositing and patterning materials in one single step. The possibility of printing over a large area may reduce the cost of production for OFETs and allow the fabrication of devices over a large area. Both conventional and new printing methods are being explored and developed by different groups. Some examples will be given below and their advantages and disadvantages will be discussed.

1. Optical Lithography. Optical lithography, also called photolithography, has been developed for more than thirty years for microfabrication of semiconductor devices.[138] Complex circuits with many layers of interconnecting lines and resolution as small as 80 nm can be fabricated using optical lithography. Photolithography is a way to transfer geometric shapes from a mask to a substrate (such as a silicon wafer). During this process, photoresist (PR) is applied to the wafer and subsequently exposed to UV light through a mask. The mask can be aligned against the substrate in a contact mode, proximity mode, or projection mode. Chemical changes occur in the exposed regions making the photoresist either more soluble (positive resist) or less soluble (negative resist) in a given solvent. The soluble part of the resist is subsequently removed leaving behind a photoresist pattern. An organic semiconductor or a metal can then be deposited on the photoresist pattern. Dissolving the photoresist pattern removes the active material above it giving the patterned semiconductor or metal. A photoresist layer can also be patterned on an unpatterned metal or semiconductor layer and used as a protecting layer when the exposed active material region is etched or dissolved away.

Patterning of the semiconducting material by photolithography can be done by directly performing lithography on the semiconductor material. This procedure has the risk of damaging the organic semiconductor as a result of either chemical degradation or physical degradation due to delamination or change of film morphology.[139] A process for pentacene patterning by lithography has been reported.[140] A water-based poly-

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(vinyl alcohol) with a chromium catalyst was used for the patterning of pentacene. The use of other organic solvents on pentacene led to delamination or morphological changes.[139] The poly(vinyl alcohol) in the photoexposed regions became water insoluble so that the unexposed regions could be removed by water to expose the pentacene underneath, which was then removed by oxygen plasma etching.[141] An alternative and less invasive method is to pattern a tall photoresist pattern on the substrate. After the semiconductor is deposited, its film breaks along the resist edges to leave isolated device areas and eliminate current leakage in the semiconductor film outside the active device areas.[142]

Both metal and conducting polymer electrodes have been fabricated using standard photolithography followed by a "lift-off" process, i.e., a dissolving photoresist removes the metal or polymer deposited above it leaving behind the desired metal or polymer patterns.[20,23,106] A lithography process has also been developed by Philips Co., the Netherlands, in which photo exposure of the conducting polyaniline converts it into an insulator.[50] A reduced complexity photolithography process was developed by Jackson's group for pentacene TFTs giving mobilities as high as 0.6 cm^2/Vs.[140]

Photolithography generally has relatively high cost per unit area. The substrate size is limited by the size of the exposure tools. It is suitable for production of high-end electronics such as computer processors and liquid crystal displays. However, for low-end applications, such as price tags and radio frequency identification tags, lower cost roll-to-roll manufacturing methods will be highly desirable.

2. Shadow Masking. Organic semiconductors and metals can be patterned through a shadow mask to form various components of OTFTs.[95] Shadow masking is a "dry" process which causes no damage to the active materials. The feature size achievable with typical commercially available stencil shadow masks is limited to about 25−30 μm. Evaporation at an angle with a culminated vapor can give feature sizes less than the feature size of the mask. However, this method requires precise control of the substrate and evaporation source positions and is undesirable for manufacturing. In addition, the size of the substrate is limited by the size of the mask. Recently, a large polymer mask was developed by 3M Co. for patterning of electrodes and organic semiconductors.[143] A set of 4−6 masks for high-performance organic integrated circuits was made by laser ablation process with the smallest feature size of 10 μm. Polymer masks are transparent, making the task of positioning the masks easier. Nevertheless, it is still a daunting challenge to do multilayer alignment of the mask over a large area. The 3M group has also developed a pentacene-based radio frequency identification (RFID) circuitry using polymer shadow masks.[9]

3. Printing. Driven by the needs of device qualities such as low cost, large area, and flexibility, significant progress has been made recently in developing suitable printing methods for the fabrication of organic TFTs.[44] Methods such as screen printing and ink-jet printing have already been widely used for the production of other devices. Applications of these methods for OFET fabrication still require new understanding and modification of the existing printing processes. At the same time, many nonconventional printing methods are also being explored by many groups.

(a) Screen Printing. Screen printing is a relatively simple printing method and has been used for printing circuit boards.[144] It has been adapted for the demonstrations of printed plastic OTFTs.[16,39,43] Typically, a specially formulated ink is squeezed through a screen mask onto the substrate surface to form a desired pattern. It was used for printing of all the active layers in organic thin film transistors.[39] Performance similar to those fabricated with photolithographically defined Au electrodes was obtained. The limitation with screen printing is the limited feature size it can print: 75 μm is the smallest feature size that is reproducible unless surface patterning is used so that the printed ink does not spread.

(b) Ink-jet Printing. Ink-jet printing (IJP) is a mature technique for printing text and pictures with high resolution. OTFTs can be printed by simply replacing conventional inks in the cartridges with specially formulated polymer solutions. High-resolution ink-jet printed all-polymer TFTs have been demonstrated.[41,122] As shown in Figure 8, the source, drain, and gate electrodes were printed with a water-based ink of the conducting poly(3,4-ethylenedioxythiophene) doped with polystyrene sulfonic acid (PEDOT/PSS). The gate dielectric is a spin-coated polyvinylphenol (PVP). The semiconducting layer is poly(9,9-dioctylfluorene-*co*-bithiophene) (F8T2). The smallest feature size achievable with IJP is usually around 25 μm without surface patterning limited by ink spreading. To achieve smaller feature sizes, hydrophobic dewetting patterns are used. The water-based PEDOT/PSS droplet splits into two halves giving a small gap in between. Using this method, the printing resolution for the channel length was reduced to as small as 200 nm.[145] The drawback is that its high-resolution low cost printing of the dewetting pattern still needs to be developed.

Printing polymer transistors has also been demonstrated by Street group at PARC.[146−149] Organic thin-film transistors were fabricated by direct patterning of solution-processable semiconductors consisting of either

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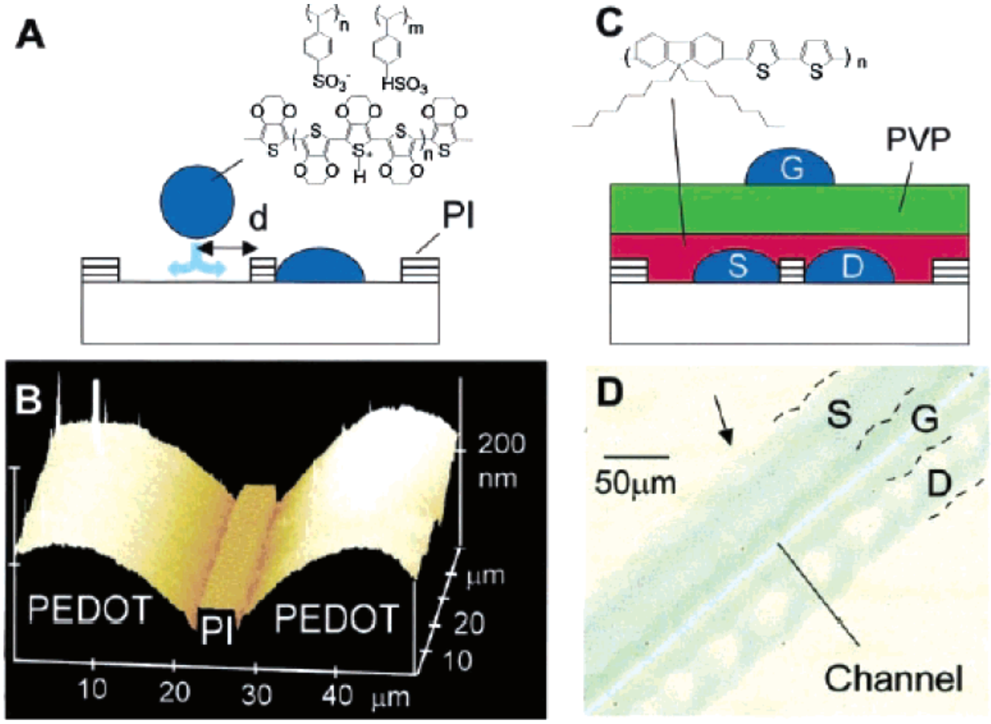

Figure 8. Schematic diagram of high-resolution IJP onto a substrate with polyimide (PI) patterns to prevent ink from spreading (A). The atomic force microscopy (AFM) image shows accurate alignment of IJP PEDOT/PSS source and drain electrodes separated by a repelling polyimide (PI) line with a channel length of 5 μm (B). Schematic diagram of the top-gate IJP TFT configuration with an F8T2 semiconducting layer (S, source; D, drain; and G, gate) (C). Optical micrograph of an IJP TFT with 5 μm channel length (D). Reprinted with permission from ref 122. Copyright 2000 American Association for the Advancement of Science.

poly(9,9′-dioctyl-fluorene-*co*-bithiophene) or a regioregular poly(thiophene).[149] Acoustic ink-jet printing was used to deposit the polymeric semiconductor onto patterned metal source−drain contacts. Printed and spin-coated transistors were found to perform identically. The regioregular poly(thiophene) exhibited a mobility of 0.1 cm^2/Vs, on−off current ratios of close to 10^6, and low threshold voltage. Alternatively, a wax layer was printed as the dewetting pattern for patterning polymer semiconductors.[150] The method has been used to fabricate small arrays of OTFTs with a regioregular poly(thiophene) and poly(9,9′-dioctyl-fluorene-*co*-bithiophene). The TFTs exhibited mobilities of $0.5-1.0 \times 10^{-3}$ cm^2/Vs and on-to-off ratios on the order of 10^4.

(c) Laser Thermal Transfer Printing. Laser imaging, otherwise known as thermal imaging, is a dry process already used for the manufacturing of digital color filters for liquid crystal displays. It is an attractive method for printing large- scale plastic electronic devices. A large variety of materials, including polymers and polymer nanoparticle composites, can be transferred using this method. The advantage of this method is that, by way of the ablative transfer of solid layers, the solvent compatibility issues can be avoided. This method was used for large-area, high-resolution, dry printing of conducting polymers as the electrodes for OTFTs.[151] In this work, two flexible films were held together by vacuum. One film was a multilayer donor and the other film was a receiver. An infrared laser beam focused onto the thin absorbing layer converted light into heat. Gas bubbles were created when the surrounding organic material was decomposed. The gas bubbles subsequently pushed the conducting layer onto the receiver. Finally, the donor and receiver films were separated, leaving patterned conductors on the receiver. Figure 9 is a schematic illustration of this process. Using a related but slightly different process, Nishio et al. made organic semiconductor thin films by excimer laser ablation (ELA) of 3,4,9,10-perylene-tetracarboxylic dianhydride (PTCDA) with ArF (193 nm), KrF (248 nm), XeCl (308 nm), and XeF (351 nm) beams.[152] They found that the thin film conductivity strongly depends on the condition of laser ablation.

(d) Microcontact Printing. Screen and ink-jet printing both have the advantage that many technological aspects of these methods are relatively well developed for applications similar to, but distinct from, organic electronics. However, currently neither has the resolution necessary for patterning the finest features that are required for useful organic circuits (typically the separation between source/drain electrodes) without using a high-resolution surface dewetting pattern. New high-resolution lithographic techniques that use elastomeric stamps and molds are also known as soft lithography.[153−155] Their use for patterning source/drain

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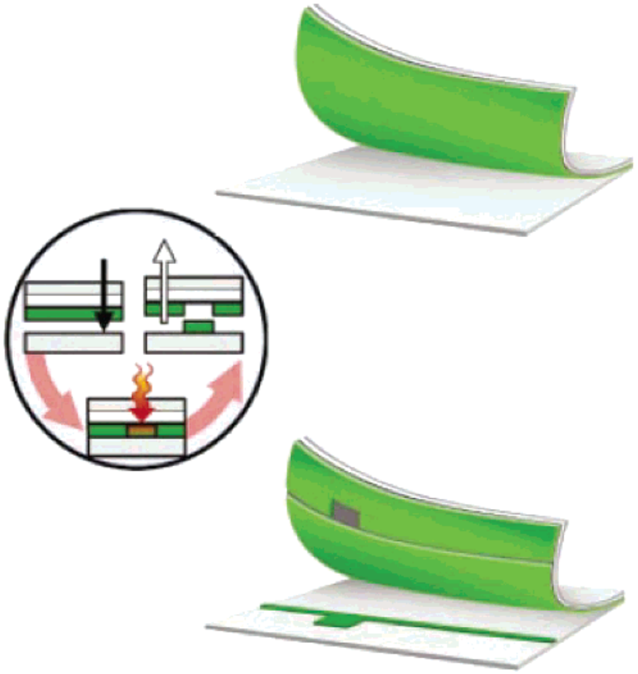

Figure 9. Illustration of the laser printing process. The two flexible films, a multilayer donor, and a receiver are held together by vacuum. The laser beam is focused onto a thin absorbing layer that converts light into heat, an optional ejection layer is placed directly underneath, and a dodecyl benzene sulfonic acid doped polyaniline (DNNSA-PANI)/single wall carbon nanotubes (SWNT) conducting layer is coated on top. The heat generated at the metal interface decomposes the surrounding organics creating a gas bubble that when expanding propels the conducting layer onto the receiver. After imaging is completed the donor and receiver films are separated. Reprinted with permission from ref 151. Copyright 2003 American Institute of Physics.

electrodes for applications in organic electronics has been demonstrated by several groups.[3,156−159] These methods are attractive because of their low cost, good compatibility with many organic materials, and demonstrated good resolution that would comfortably satisfy the requirements for nearly all realistic applications of organic electronics. Although many aspects of these techniques are less developed than those of screen and ink jet printing, research applications of them have been shown the patterning of a wide range of materials ranging from biological molecules, to organic polymers, and to metals.

Microcontact printing is one of the most commonly used soft lithography methods.[160] In a microcontact printing process, molecular transfer or a contact-induced chemical change of the surface occurs. The nanoscale interaction between substrate and stamp enables transfer of materials from a stamp to a substrate. The resolution of microcontact printing is associated with the modulus of the elastomer used for the preparation of the stamp.[161−163] Feature sizes as small as a few tens of nanometers can be microcontact printed.[162] This method has been used to pattern Au and Ag drain and source electrodes of OFETs.[3,156] It was also used to pattern solution-deposited semiconductor by microcontact printing a hydrophilic and hydrophobic pattern where the semiconductor is selectively deposited only on the hydrophilic regions.[164] Recently, microcontact printing was used to print a hydrophobic silane layer on a flexible plastic substrate.[165] The subsequent electroless plated Ni gate electrodes were only deposited at regions without the silane layer. Flexible integrated circuits were demonstrated in this work.[165]

(e) Embossing. Embossing is a way to imprint features in thermoplastic materials and polymer solutions or nanocomposites.[154,155] One example of application of this method in industry is the manufacturing of compact disks. Embossing performed with a liquid ink is also called "micromolding". In this case, a patterned elastomer stamp is pressed onto the liquid, which is subsequently dried or solidified. Peeling off the stamp leaves the negative image of the stamp in the dried liquid. Conducting polymer electrodes and graphite ink were molded into drain and source electrodes for OFETs.[157]

When used to print directly on a thermoplastic material with a hard master, embossing is also called "microcutting".[166,167] PEDOT drain and source electrodes can be microcut on poly-(ethylene terephthalate) (PET) substrates.[168] As shown in Figure 10, a polymer substrate was coated with thin ceramic or polymeric layers. A hard master with sharp, protruding features is used to microcut the coated layers into regular structures. Single or multiple microcutting can be performed. Recently, self-aligned, vertical-channel OTFTs have been demonstrated using embossing techniques.[169]

(f) Cold Welding. Cold welding refers to metallic bond formation between two metal surfaces when a pressure is applied. This method was applied to the micropatterning of organic light-emitting diodes[170,171] and OFETs.[172] In this process, a rigid stamp made of silicon is first coated with a thin layer of adhesion-reduction layer followed by Au metal. It is then pressed with high pressure (50−150 MPa) onto the surface of an unpatterned film of Au on organic semiconductor. The Au in the protruded regions of the stamp is transferred as the

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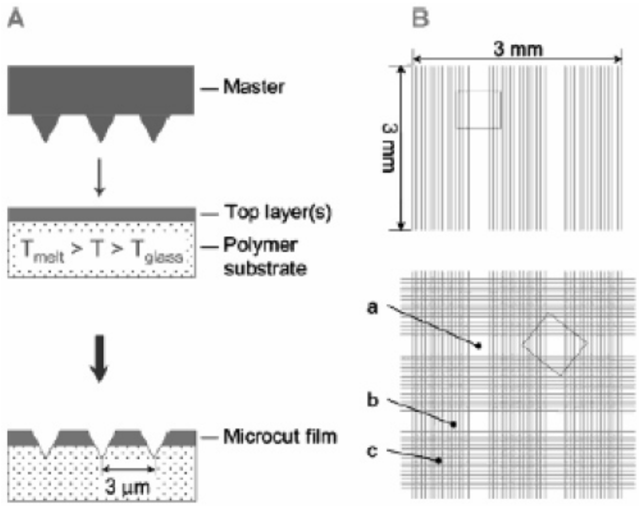

Figure 10. Schematic diagram of the polymer-substrate supported microcutting process. (A) Thin ceramic or polymeric layers coated onto a polymer substrate were embossed with a master comprising sharp, protruding geometries while the substrate is in its solid state. The top layers were microcut into regular structures. (B) Top view of the resultant microcut multilayers: (a) unstructured areas, (b) single cut, and (c) doubly cut areas. Reprinted with permission from ref 168. Copyright 2002 Wiley−VCH.

electrodes. The thin Au layer between the drain and source is removed by Ar sputter etching. Transistors with channel length ranging from 85 to 245 nm were fabricated and showed performance similar to those with photolithographically defined electrodes.[172]

(g) Soft Lamination of Electrodes. Bottom-contact device structure is preferred when extensive processing steps are needed for patterning the drain and source electrodes so that these procedures do not degrade the organic semiconductor. However, bottom-contact devices tend to have worse performance than top-contact devices because organic semiconductors tend to form small grains on metal electrodes and lead to higher injection barriers.[127] Top-contact, on the other hand, gives more robust and larger contact areas. But it is hard to perform “wet” processing procedures directly on organic semiconductors. In addition, hot metal atoms deposited on the organic semiconductor also cause damage to the semiconductor, resulting in higher injection barrier. Lamination of electrodes onto the semiconducting layer avoids all the above issues. In this case, patterning of the electrodes is carried out independently on a substrate which is subsequently laminated onto another substrate already coated with the gate, dielectric, and semiconductor to complete the transistor structure. A soft lamination approach was recently reported, in which a elastomeric polydimethylsiloxane (PDMS) substrate was used to support the electrodes.[173] Owing to its elastomeric properties and extremely flat surface, PDMS can adhere to other flat substrates spontaneously upon contact. Therefore, no pressure or adhesive layer is needed to ensure that the two substrates are held together intimately. Transistor arrays on plastic substrates can be fabricated using microcontact-printed Au drain and source electrodes on PDMS. The PDMS substrate also serves as a protecting layer for the active materials. The laminated transistors can be soaked in a soap solution without any alterations in their electrical characteristics.[173] Additional moisture and oxygen barriers can be easily applied to the device without damaging the organic semiconductor during encapsulation. The laminated devices also have greater mechanical strength. The active layers are in a mechanically neutral plane and therefore do not crack even when bent into high curvature. The bendability of such devices is thus limited by the plastic substrate rather than the mechanical properties of the semiconductor, electrodes, and the dielectric layer.[173]

The above soft lamination approach requires patterning of metal electrodes on PDMS. Patterning on PDMS is not a trivial task because PDMS is soft and swells easily when in contact with many common organic solvents, causing distortion of its features. Deposition of metal on PDMS has to be done with minimum heating of the substrate. Otherwise, cracks will result in the metal films due to the low glass transition temperature (T_g of 150 K) and large thermal expansion coefficient of PDMS. Several approaches have been reported for the patterning and metallization of PDMS. A simple method for patterning metal electrodes on PDMS is to use PDMS to replicate the desired patterns followed by direct deposition of metal onto the PDMS. The metal layer in the protruding regions is then used to form electrical contacts. The metal layer can be etched slightly so that the adjacent electrodes are not shorted. OFETs with channel length as small as 100 nm can be fabricated using this method.[174] Other types of devices, such as organic light-emitting diodes[175,176] and memory devices,[177] have also been fabricated using this method.

Another PDMS metallization method relies on tuning the surface chemistry of the outer surface of the stamp and substrate so that a chemical reaction between the two surfaces leads to the transfer of the desired layer. For example, both Ti and PDMS stamp surfaces can be treated with oxygen plasma for a few minutes to give −OH derivatized surfaces. Bringing these two surfaces into contact results in a chemical reaction to form a Ti−O−Si bond that facilitates the transfer process.[178] A metal stack of Au and a thin Ti above it patterned by photolithography can be transferred onto a PDMS stamp using this surface chemistry.[178] OFETs can be fabricated using similar surface chemistry with slightly modified procedures.[179] Alternatively, SiO_2 dielectric surface can be modified with a “glue” layer of 3-mercapto-propyltrimethoxysilane. In such a case the oxide surface is covered with thiol (−SH) groups which can bind with Au electrodes on the protruded regions of a stamp surface. When the PDMS stamp is pulled away, the bound gold electrodes stay attached to the thiol groups as shown in Figure 11.[178]

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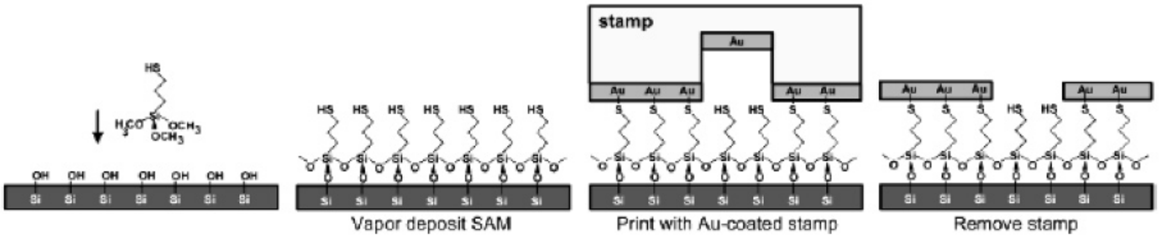

Figure 11. Surface chemistry for soft lamination of electrodes. Reprinted with permission from ref 178. Copyright 2002 American Chemical Society.

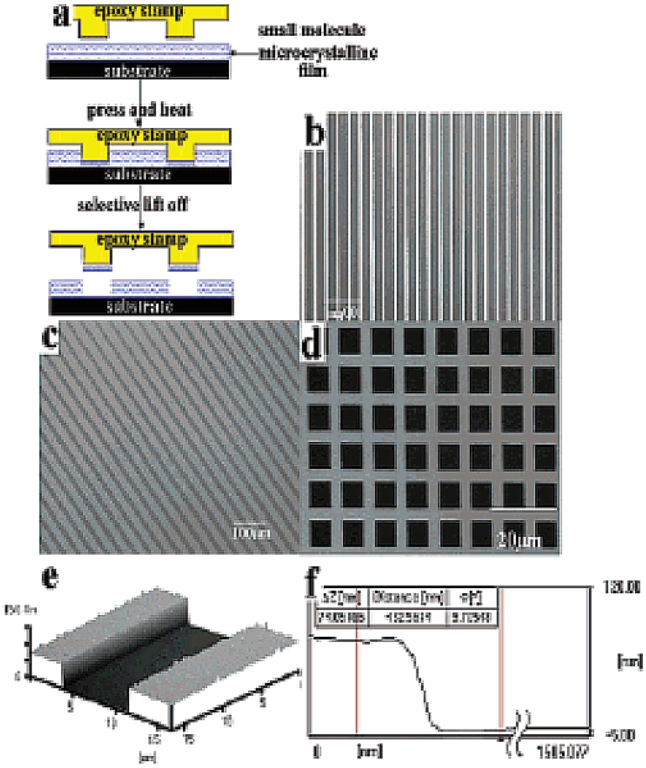

Figure 12. (a) Hot lift-off process. Optical micrographs of the microstructures of several organic semiconductor microcrystalline films: (b) CuPc/Si, (c) Alq_3/NPB/ITO, and (d) H_2Pc/Si. (e and f) Cross-sectional analysis of AFM image showing the morphology perpendicular to the edge of CuPc microcrystalline film pattern. Reprinted with permission from ref 181. Copyright 2003 American Chemical Society.

Using this approach, high-performance organic transistors have been reported by soft-contact lamination of source/drain electrodes supported by gold-coated high-resolution rubber stamps against organic semiconductor films.[180] The contact resistance of the laminated contacts with organic semiconductors such as pentacene (p-type) and copper hexadecafluorophthalocyanine (n-type) were examined. It was shown that the parasitic resistances related to the laminated contacts are much smaller than those associated with contacts formed by deposition of gold electrodes right on top of the organic active layer.

(h) Hot Lift-Off. “Hot lift-off” is a subtractive method for micropatterning of organic semiconductors. In this method, a patterned epoxy stamp is pressed onto the organic semiconductor and heated. Upon removal of the stamp and the semiconductor that was in contact with it, a patterned semiconductor layer is left behind as shown in Figure 12.[181] Small molecular materials, such as copper phthalocyanine (CuPc), metal-free phthalocyanine (H_2−Pc), *N*,*N*′-di(naphthalen-1-yl)-*N*,*N*′-diphenylbenzidine (NPB), and tris(8-quinolinolato)aluminum (AlQ_3) were successfully patterned using this approach.[181]

(i) Selective Electrical Polymerization. Conducting polymer electrodes can be formed by direct polymerization from their monomer solutions. All-organic thin-film transistors can be patterned by selective polymerization.[182] By electrochemical polymerization of doped PEDOT from a solution containing its monomer and poly(styrene sulfonate) (PSS) sodium salt, source and drain contacts were formed on the anode. The polymer electrode patterns were subsequently transferred to a polyamide support followed by the depositions of organic semiconductor, dielectric layer, and a gate electrode. Such a method resulted in a mobility of 0.01 cm^2/Vs for pentacene transistors.

IV. Summary and Future outlook

The field of organic transistors has witnessed much exciting progress in the past few decades. The mobilities of several organic semiconductors are already similar to or even better than that of amorphous-Si transistors. To move the field forward, there are a few pressing issues to be addressed. First, it is important that a “killer application” is identified. In terms of performance, it is difficult for organic transistors to compete with existing poly-Si transistors. The key advantages of organic transistors lie in their low-cost fabrication over a large area and compatibility with lightweight plastic substrates. Applications such as electronic paper and RFID tags are likely promising applications suitable for organic transistors. Issues related to manufacturing these devices are yet to be addressed. Second, there is still a lack of good understanding of various parameters that control the semiconductor film morphology. Better understanding of the organic semiconductor growth mechanism and the effect of substrate surfaces will undoubtedly enable better device performance. Third, better understanding of the organic transistor degradation mechanism is needed. There have been only limited studies on this general topic.[183] Understanding the degradation mechanisms and applying proper encapsulation methods will be crucial for implementing

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organic transistors in practical devices. Finally, truly low-cost manufacturable roll-to-roll fabrication methods for printing complex circuits need to be demonstrated.

In summary, promising progress has been made in designing new organic semiconductors and understanding their processing parameters, as well as developing low-cost patterning methods. There are still some critical issues to be addressed before organic transistors can be used for commercial purposes. Nevertheless, the future of organic transistors is bright.

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